Design of CMOS Fractional-N PLL

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I. Introduction

Nowadays, many system-on-chip (SoC) applications are required to operate at very high frequency. The higher operating frequencies, the more difficult task to generate and distribute clock signals. By using a PLL, it is possible to generate a high frequency clock signal from a low frequency, stable external clock signal. One more benefit is that the divider of PLL can be programmed to generate clock signals at many frequencies that are multiple of external reference clock frequency, this increases the flexibility for clock generators.

This paper presents a fully integrated fractional-N PLL used for clock generator. The PLL is designed using Samsung 0.13um CMOS process with a supply voltage of 1.2V. The input reference clock range is from 10MHz to 40MHz. It can be programmed to generate a rail-to-rail output clock from 2.2GHz to 2.6GHz.

II. System level block diagram

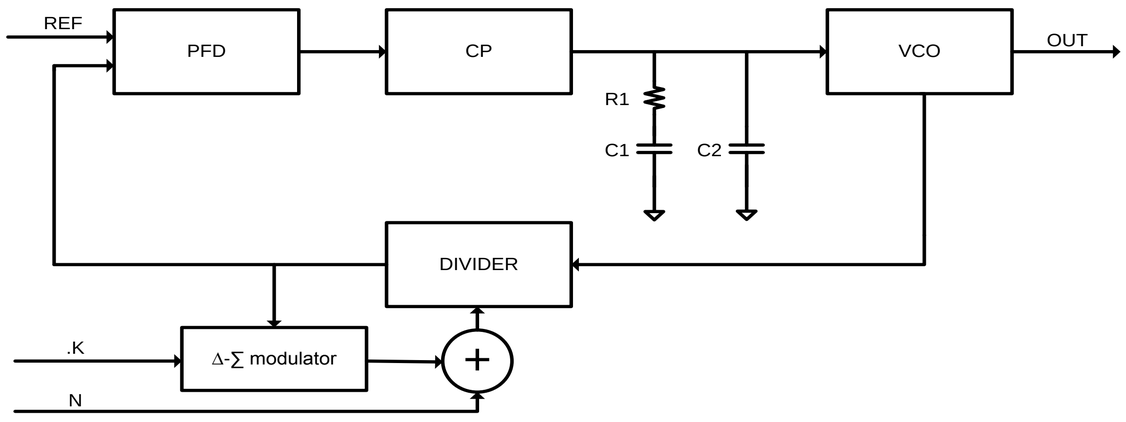

Figure 1. System level block diagram

A tri-state phase frequency detector (PFD) is used to compare the phase of feedback signal from divider output to that of reference signal. The error signal generated from PFD is used by the Charge Pump (CP) to add, remove charge from loop filter. The output voltage of loop filter is used to control the voltage-controlled oscillator (VCO). The divider scales down the frequency of VCO output and then feedbacks the signal to PFD. MASH111 is used for delta-sigma modulator to shape the quantization noise.

III. Voltage-controlled Oscillator

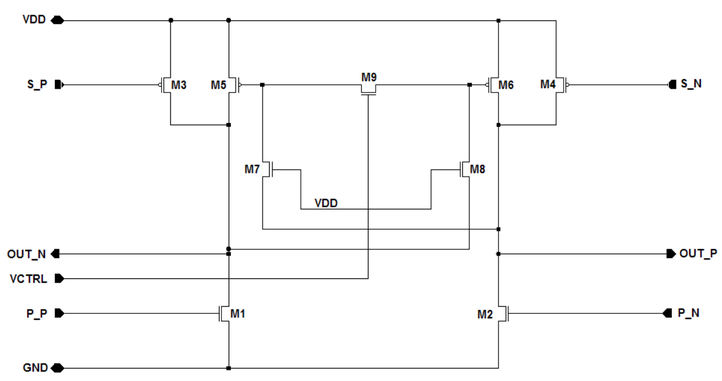

Figure 2. Saturated-delay cell

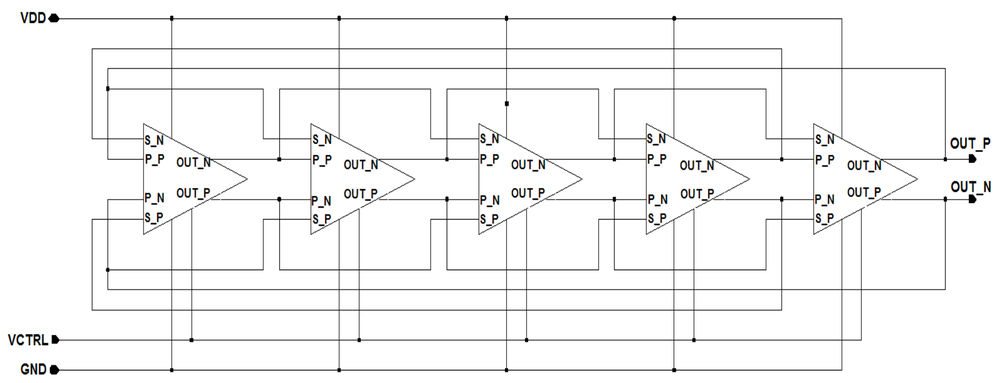

Figure 3. 5-stage ring VCO

The VCO is a 5-stage ring VCO, using feed-forward technique and saturated delay cells to archive high oscillation frequency and low phase noise. The tuning range is from 2.2GHz to 2.6GHz, VCO gain Kvco=850MHz. The VCO can archive a phase noise of -104.2dBc/Hz at 1MHz offset when output frequency is 2.4GHz.

IV. Delta-sigma Modulator

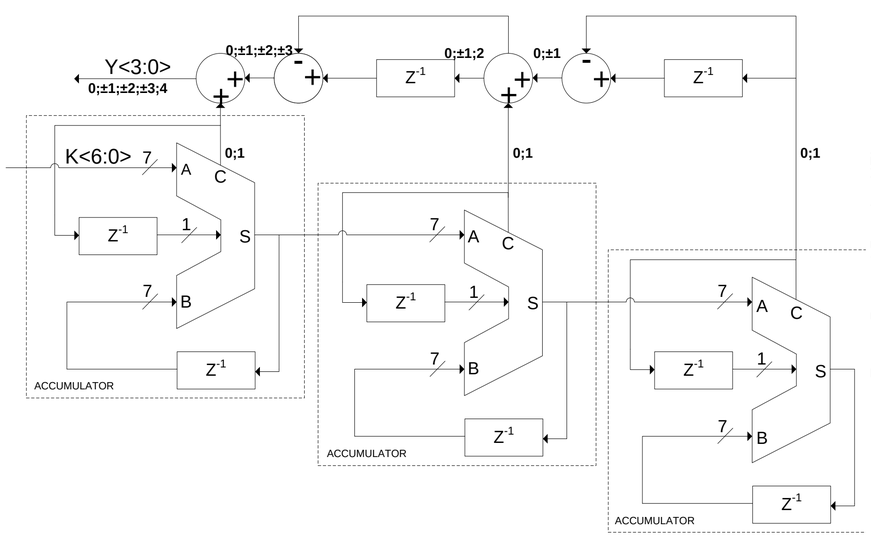

Figure 4. MASH111 Structure with modified accumulator

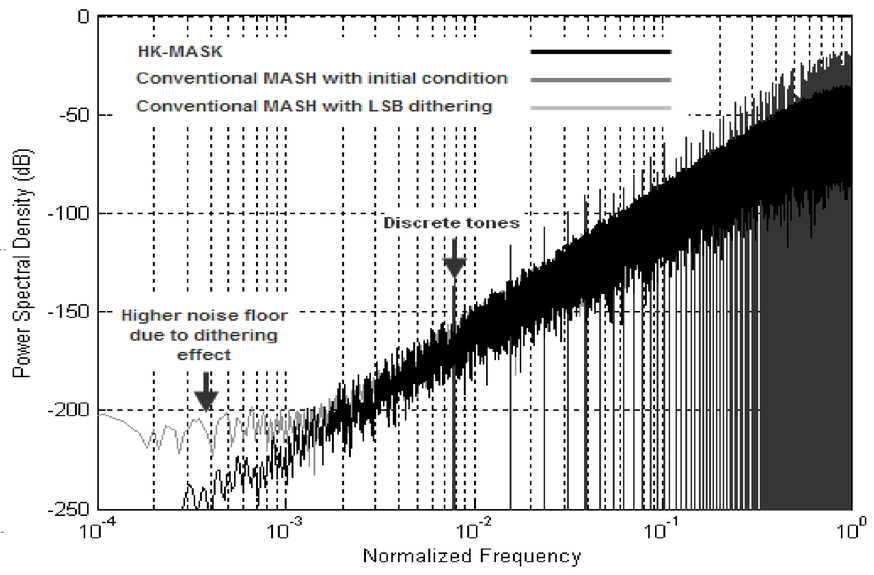

Figure 5. Power Spectral Density

Delta-sigma modulator uses MASH 1-1-1 structure, each stage is a 7-bit accumulator with carried-out bit feed back to the adder (HK-MASH). This structure shows better discrete tones suppression as well as low noise floor.

V. Performance

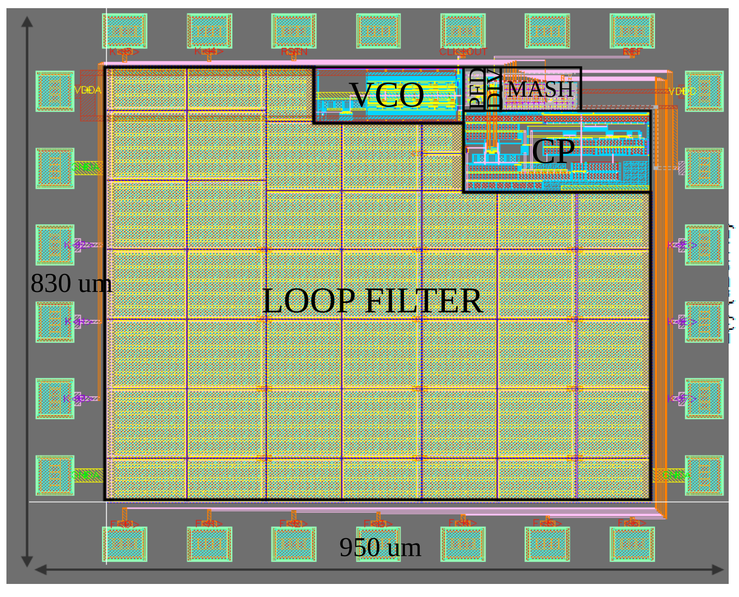

Figure 6. PLL layout

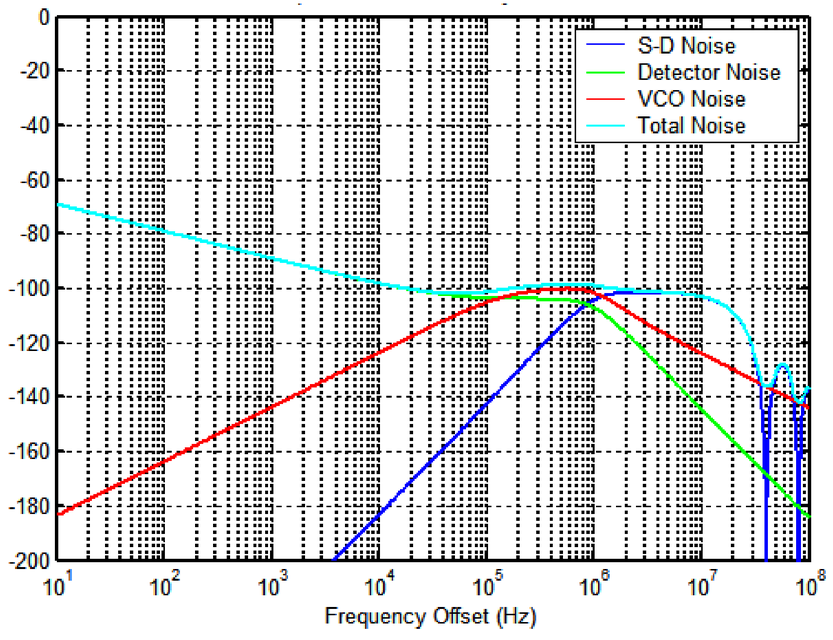

Figure 7. Phase noise analysis

Parameter	Value
Supply Voltage	1.2V
Output frequency range	2.2GHz – 2.6GHz
Phase noise (@2.4GHz)	-100dBc/Hz (@1MHz offset)
Lock time	<10 µs
Power	50mW
Silicon area	950µm x 830µm

VI. Conclusions

The PLL is designed using Samsung 0.13um CMOS process. The simulation results show that it can generate clock frequency in the range from 2.2GHz to 2.6GHz, with a phase noise of -100dBc/Hz. The PLL is fully integrated and suitable for on chip clock generator.

References

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