Series-Biased CMOS Power Amplifiers Operating at High Voltage for 24 GHz Radar Applications

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I. Introduction

Series-bias technique allowed overcoming the low voltage constraint of scaled-down CMOS technology, providing practical solution for realizing high power CMOS amplifier. A two-stage amplifier employing the series-bias technique of four cascode power cells showed a maximum small-signal gain of 25.6 dB, an output power of 20 dBm, and a PAE of 12.5 % at 21 GHz. This is the first CMOS power amplifier delivering 100mW output power above 20 GHz. A three-stage series-bias amplifier having common-source transistor showed a small-signal gain of 17.3 dB, an output power of 17.5 dBm, and a PAE of 8.8% at 23.5 GHz. These amplifiers employing the series-bias technique are shown to have a highly favorable FOM compared to the results obtained from conventional amplifiers.

II. 2-stage Series-biased Amplifier with Cascode Transistors

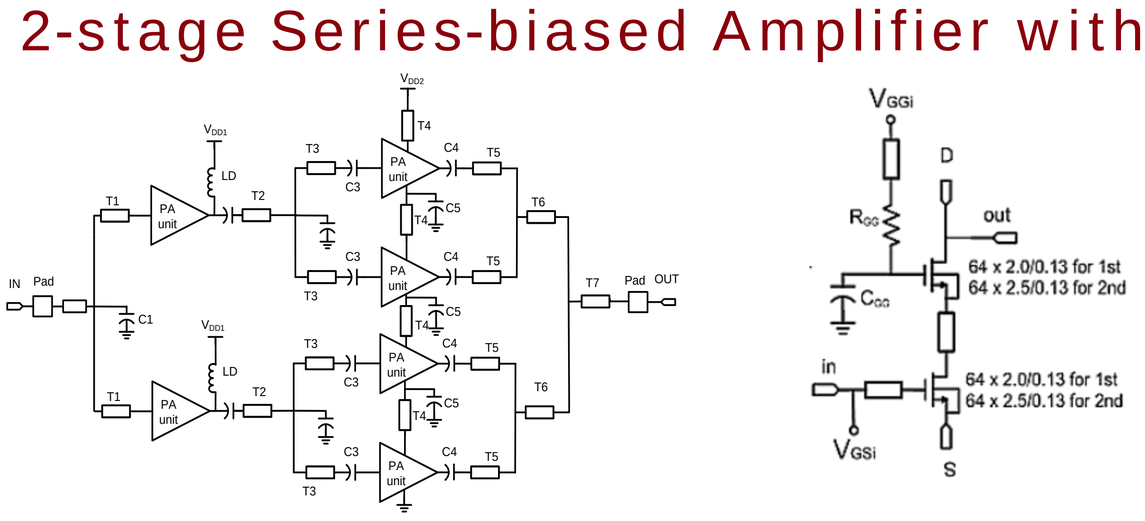

Fig. 1 (a) Schematic of series-biased CMOS power amplifier using 0.13 um RFCMOS process. (b) Cascode power cell, the transistor size is 64×2um and 64×2.5um for 1st and 2nd stage, respectively.

The supply voltage of the current scaled-down CMOS technology is now about 1 V, and the low supply voltage impose a serious constraint on the design of a high power CMOS power amplifier. By using the high supply voltage and low operating current, the loss from DC-to-DC conversion as well as Ohmic loss could be reduced.

In CMOS technology, an output power of 33 dBm was achieved at 1.9 GHz by stacking four MOSFETs. However, high-voltage CMOS power amplifier implementation has not been investigated at frequency above 20 GHz. Therefore, there is a lot of research interest in achieving high output power level using CMOS process.

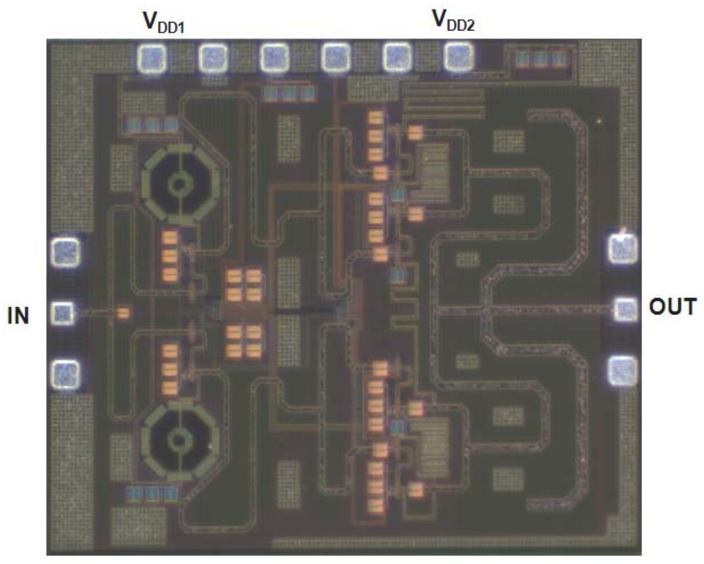

Fig. 2. Photograph of the 2-stage series-biased CMOS power amplifier having cascode PA unit, the chip size is 1.4 × 1.2 mm2

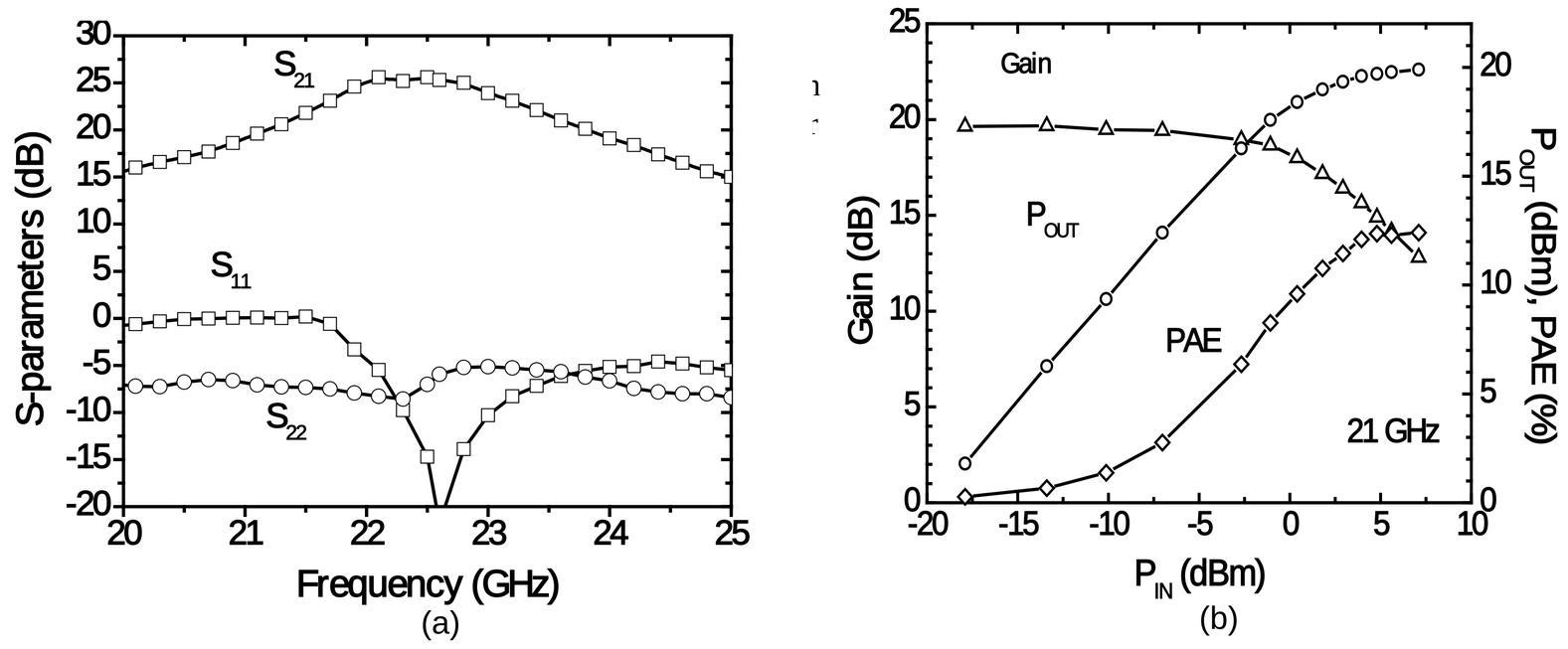

Fig. 3. Measured (symbol) and simulated (line) results of 2-stage series-biased CMOS power amplifier when biased at total current of 67 mA, (VDD1 = 2.6 V and VDD2 = 12 V).
(a) S-parameter, a maximum small signal gain 25.6 dB achieved without pad de-embedding (b) Large-signal performance, 20dBm saturated output power of 12.8 dB power gain at PAE of 12.4%.

III. 3-stage Series-biased Amplifier with Cascode Transistors

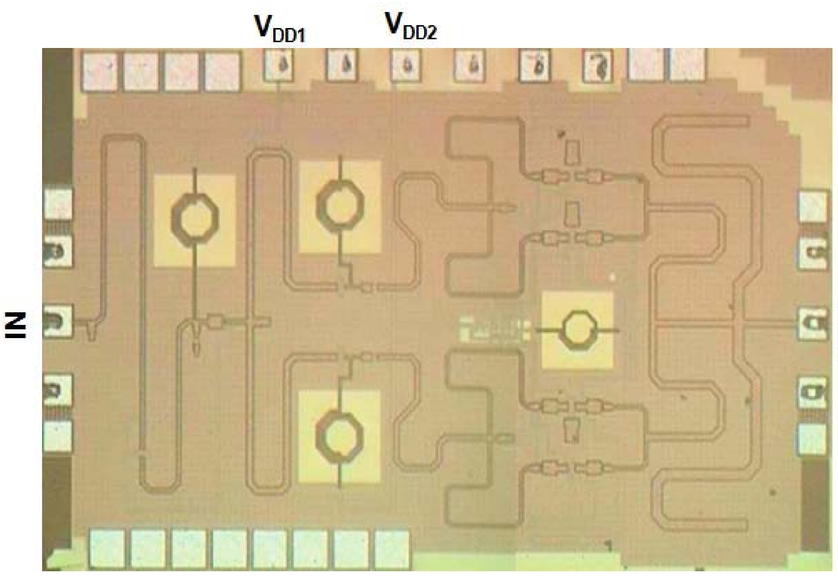

Fig. 4. Photograph of the 3-stage series-biased CMOS power amplifier having cascode PA unit, the chip size is 1.8 × 1.1 mm2

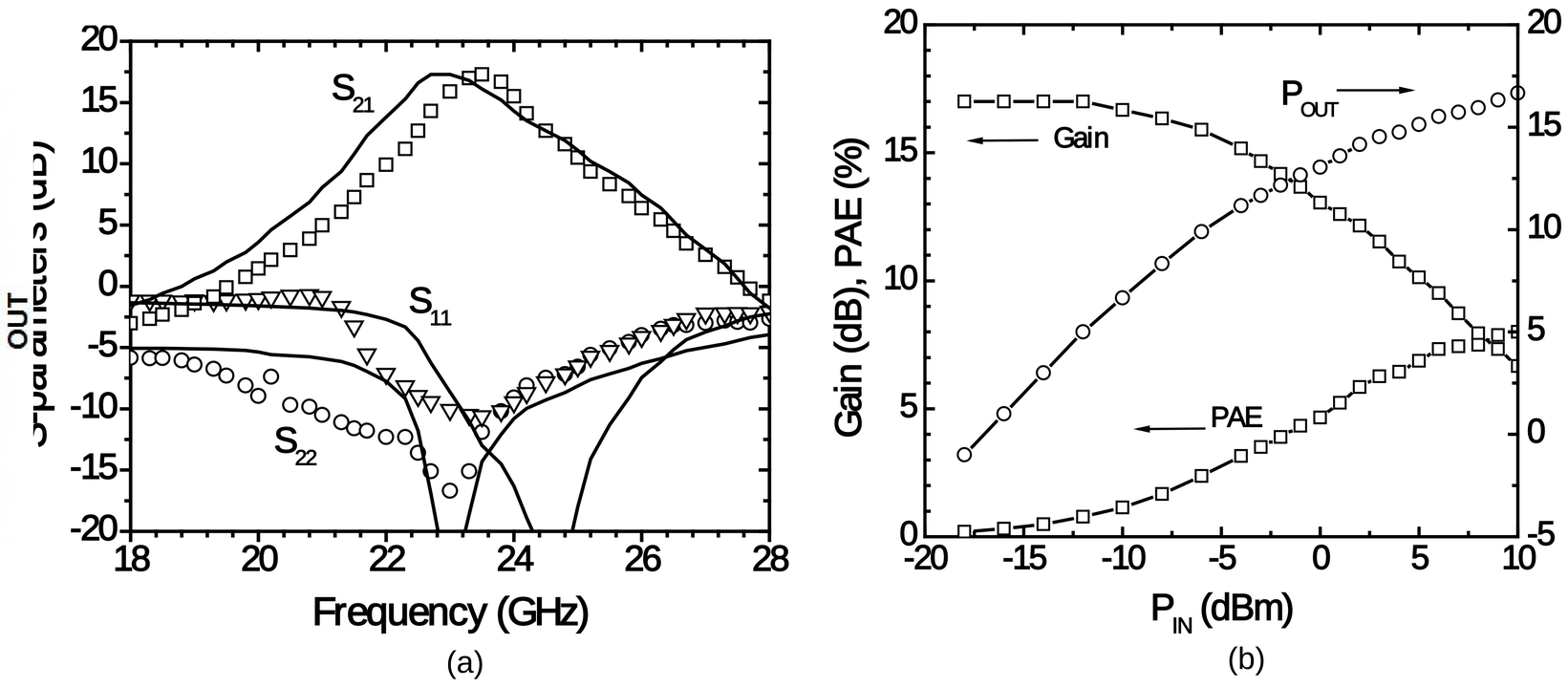

Fig. 3. Measured (symbol) and simulated (line) results of 2-stage series-biased CMOS power amplifier when biased at total current of 86 mA, (VDD1 = 1.8 V and VDD2 = 8 V).
(a) S-parameter, a maximum 17.3 dB small signal gain and approximately 2GHz 3dB bandwidth (b) Large-signal performance, saturated output power 17.5 dBm of PAE around 8.8%.

VI. Conclusions

CMOS power amplifiers based on series-biased technique demonstrated, the measured results showed effectiveness of this approach to overcome the low voltage and low output level of the CMOS power amplifier. The series-bias technique combined with cascode configuration effectively increased the operating voltage of the amplifier and achieved a 100 mW output power level above 20 GHz using CMOS technology. The results will be useful for fully integrated microwave/millimeter-wave transceivers in standard CMOS technology.

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