A Nano-Watt Low-Drop-Out Voltage Regulator for UHF RFID Tag IC

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Introduction

This work focuses on the low-drop-out (LDO) voltage regulator for an ultra-high-frequency (UHF) passive tag operating at 900MHz. To increase the sensitivity of passive tag to -10dBm, the design priority needs to be concentrated to lower the power consumption of building blocks in the tag. Besides, there is a period – a ten of microseconds- where the RF power is absent [1]. Thus, it demands an ultra low power for the voltage regulator, which is presented in this paper.

Design Implementation

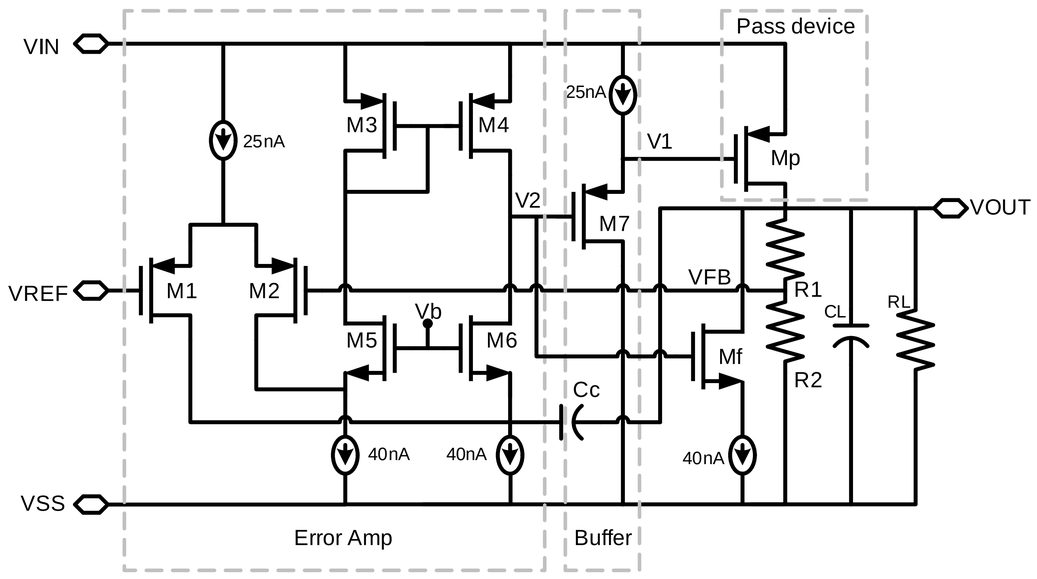

Fig. 1. Schematic of LDO voltage regulator.

As the most conventional LDO voltage regulator, the proposal structure consists of the error amplifier, the buffer, and pass device as shown in Fig.1. The desired output voltage is 1.2V to supply the load current about 60uA for the digital and analog part of UHF-band RFID tag IC. Owing to the low output impedance of buffer, P_1 at V_1 is pushed out for several decades beyond the UGF. Therefore, the analyzing of the voltage regulation can be realized as two poles system consisting P_0 and P_2 at V_2 and V_{OUT}, respectively.

There are two kinds of compensation techniques, which are employed in the proposal circuit: current buffer Miller and feed-forward transconductance. The coupling capacitor C_C and M_6 act as the current buffer Miller compensation to split P_0 at V_{OUT} and P_2 at V_2 to achieve the stability in the full range of load current [2]. However, it is worst to mention that the current buffer Miller compensation generate third pole P_3. This pole is not desired and usually pushed beyond UGF by large C_C and gm_6 which trade off to both of area(Tag IC cost) and power(Tag input sensitivity). Otherwise, the combination of P_2 and P_3 at high load current turns into a high Q-factor conjugate complex pole, which degrades the stability and settling time of regulator. In order to overcome this issue, a feed-forward transconductance M_f is added into the circuit to reduce the Q-factor [3]. In addition, the feed-forward M_f does not require high power since it can reuse the bias current for M_P. Indeed, it is required to supply a small current through M_P during the low load current. R_1 and R_2 are designed to be function as the simple voltage divider, and then the current through them can be kept as low as several nano-amperes.

Chip implementation and results

Fig.2 shows the fabricated UHF-band RFID Tag IC in the 0.18-µm CMOS process. The regulator has been integrated with other analog blocks and digital part in order to fully verify the functionality. The analog blocks include voltage multiplier, bias generator, demodulator and modulator, power-on-reset and clock generator. The digital has been implemented following Gen 2 specification. The regulator drives an on-chip decoupling capacitance is 250pF, which is the main storage for RFID tag IC. The design was verified with the input voltage in range 1.4V to 2.2V and load current of digital part from 1uA to 60uA. The total current consumption including bias voltage generation is 220nA@1.4V.

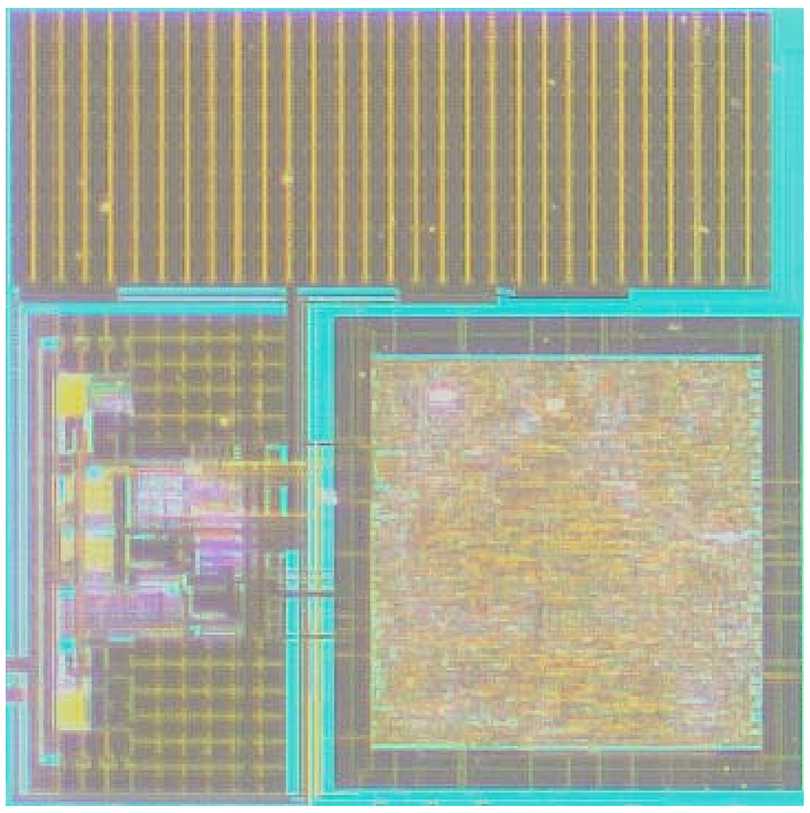

Fig.2. Fabricated UHF-band RFID Tag IC in 0.18-µm CMOS process

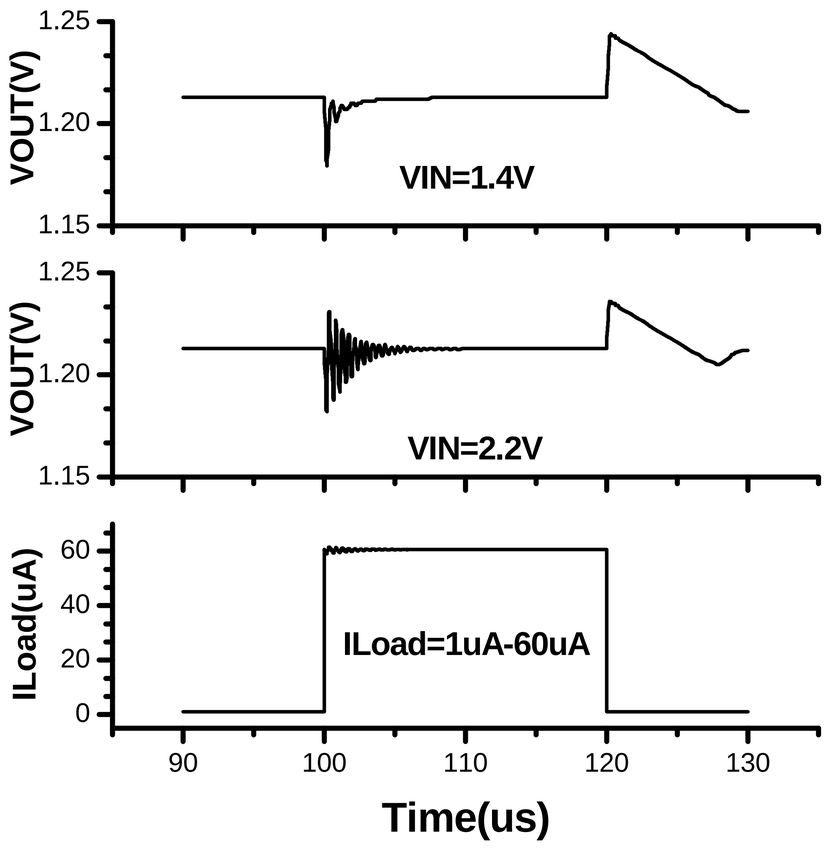

Fig. 3. Transient response.

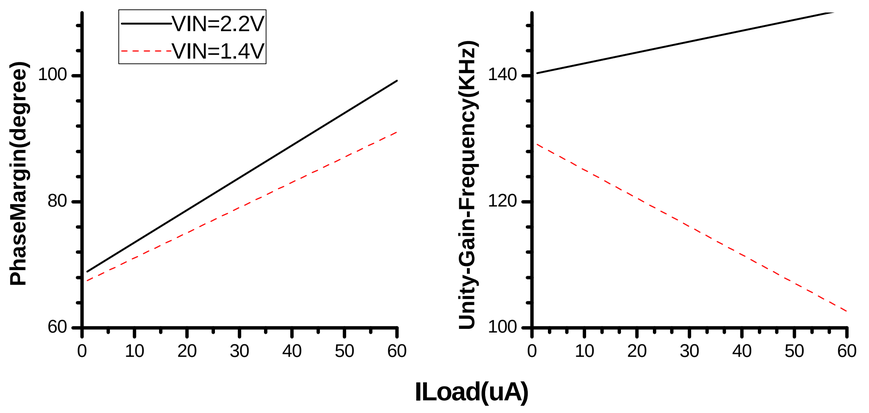

Fig. 4. Phase Margin and UGF at different load current and input voltage.

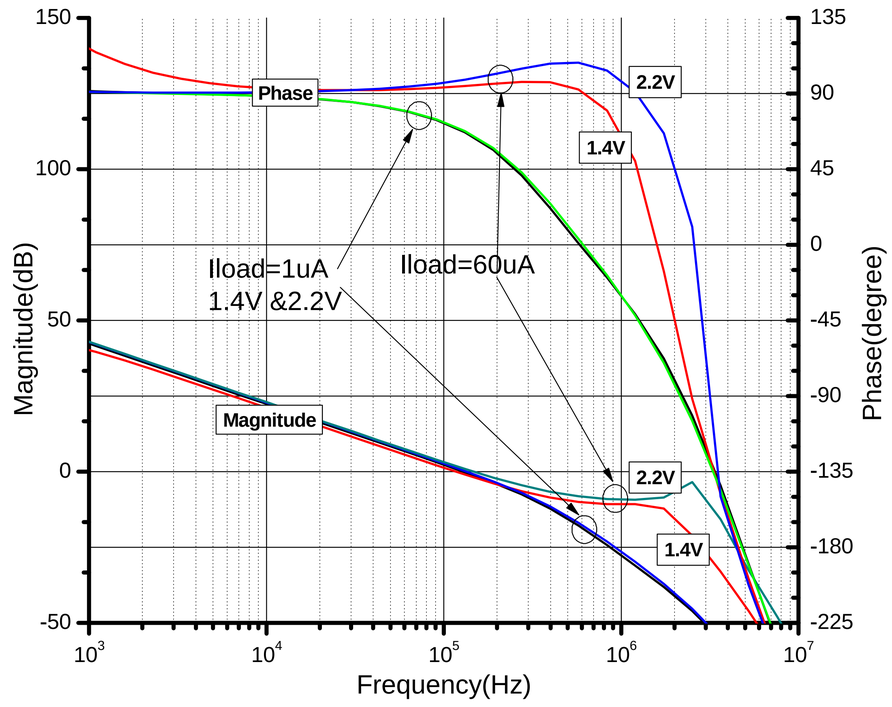

Fig. 5. AC response of loop-gain under various load current and input voltage.

The design was verified with the input voltage in range 1.4V to 2.2V and load current from 1uA to 60uA. The on-chip decoupling capacitance is 250pF, which is the main storage for RFID tag IC. The simulation results show that the regulator functions properly in the expected working range of input voltage and load current (Fig.3 - Fig.5).

The total current consumption including bias voltage generation is 220nA@1.4V. The layout size is 60um x 40um in 6-metal 0.13um CMOS process (Fig.6).

Acknowledgement

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Reference

[1] EPCglobal, "EPC radio-frequency identity protocols Class-1 Generation-2 UHF RFID air interface version 1.0.9," 2005.

[2] Mohammad Al-Shyoukh et al, "A Transient-Enhanced Low-Qui-escent Current Low-Dropout Regulator With Buffer Impedance Attenuation," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1732-1742, Aug. 2007.

[3] Hoi Lee et al, "Active-Feedback Frequency-Compensation Technique for Low-Power Multistage Amplifiers," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, Aug. 2003.

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